RumRaisin on Chip (RRoC)

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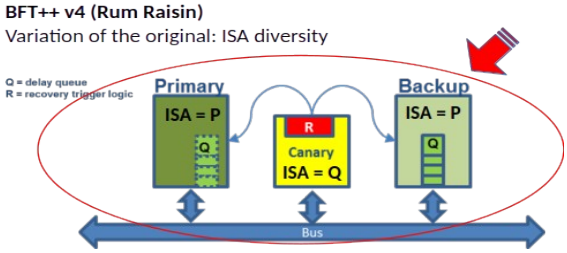
With the increasing prevalence of ``drive by wire", electronic systems like advanced driver-assistance systems (ADAS) and electronic control units (ECUs) are taking over more and more critical roles in the functionality and safety of modern day vehicles. Unfortunately, as highlighted in many real life events [1][2]. This trend also means increased safety risk from any malfunction in these components. In response, the ISO 26262 was proposed as a systematic approach for managing functional safety throughout the development lifecycle of automotive electrical and electronic systems. In particular, ISO 26262 defines the Automotive Safety Integrity Levels (ASIL) to combine the probability of exposure to hazard, the extent to which it is controllable by a driver, and the severity of failure to control such hazard. ASIL-D is the highest level of integrity defined under ISO 26262. In order to attain ASA standard approach for achieving ASIL-D is to have redundant hardware components operating on the same inputs and flag any discrepancy in their output as an error condition. A popular implementation of this idea is the dual-core lockstep configuration (DCLS), a system needs to satisfy a system requirement of having fewer than 1% single point of failure. Unfortunately, since ISO 26262 (and thus ASIL) only focuses on random, unintentional faults, existing ASIL-D compliant systems are unlikely to provide any defense against the much more dire threat from cyberattacks. This is because in the face of a cyberattack, all the redundant components will be processing the same malicious input, and thus reaching the same compromised state, which will be passed as normal by any fault tolerance mechanism (common ode failure).

In order to extend ASIL-D compliant systems to achieve any safety guarantee against cyberattacks, we need an approach that is i) scalable in both the class of attacks and the size of software that can be covered, ii) cheap to deploy in both hardware and performance cost, and iii) provides high safety, security and compatibility guarantee. The scalability requirement precludes fault avoidance methods that use formal methods to identify and remove all security problems in software. The stringent performance requirement precludes many software based security monitoring solutions (which can have >5% performance overhead).



BFT++ family of methods [3,4] can easily provides cyber-attack tolerance as well as fault tolerance. A variant of BFT++, called RumRaisin uses ISA diversity to defends against cyber-attack while providing fault tolerant. It will surpass ASIL-D requirement and provide additional safety of cyber-attack resilience with stateful program execution recovery (warm recovery). Rum Raisin uses 2 different processor instruction set architectures (ISAs), and configure them in BFT++ fashion, as such if one of the particular ISA core is attack, the other ISA core will crash, hence an attack is detected, and stateful recovery can immediately be initiated, using the delayed state of the backup core.

GaTech is proposing to develop a prototype of RRoC and evaluate its efficacy against faults and cyber-attacks. We will develop RRoC with three cores using two distinct instruction set architectures RISC-V and MIPS, on an FPGA. We will evaluate and demonstrate that RRoC is resilient against farious cyber-attacks as well as faults. While the development of RRoC was initially motivated by automotive safety & security, RRoC is largely applicable to general CPS applications with high safety and security requirements, including that of energy infrastructure.

References:

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