BIRD - ICRDE Project Extension:

RumRaisin on Chip

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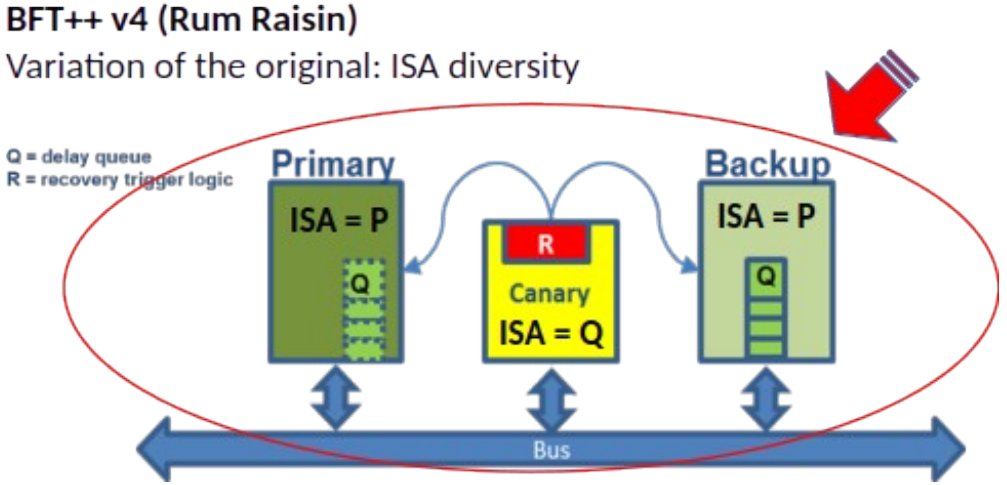
Problem Statement (motivation)

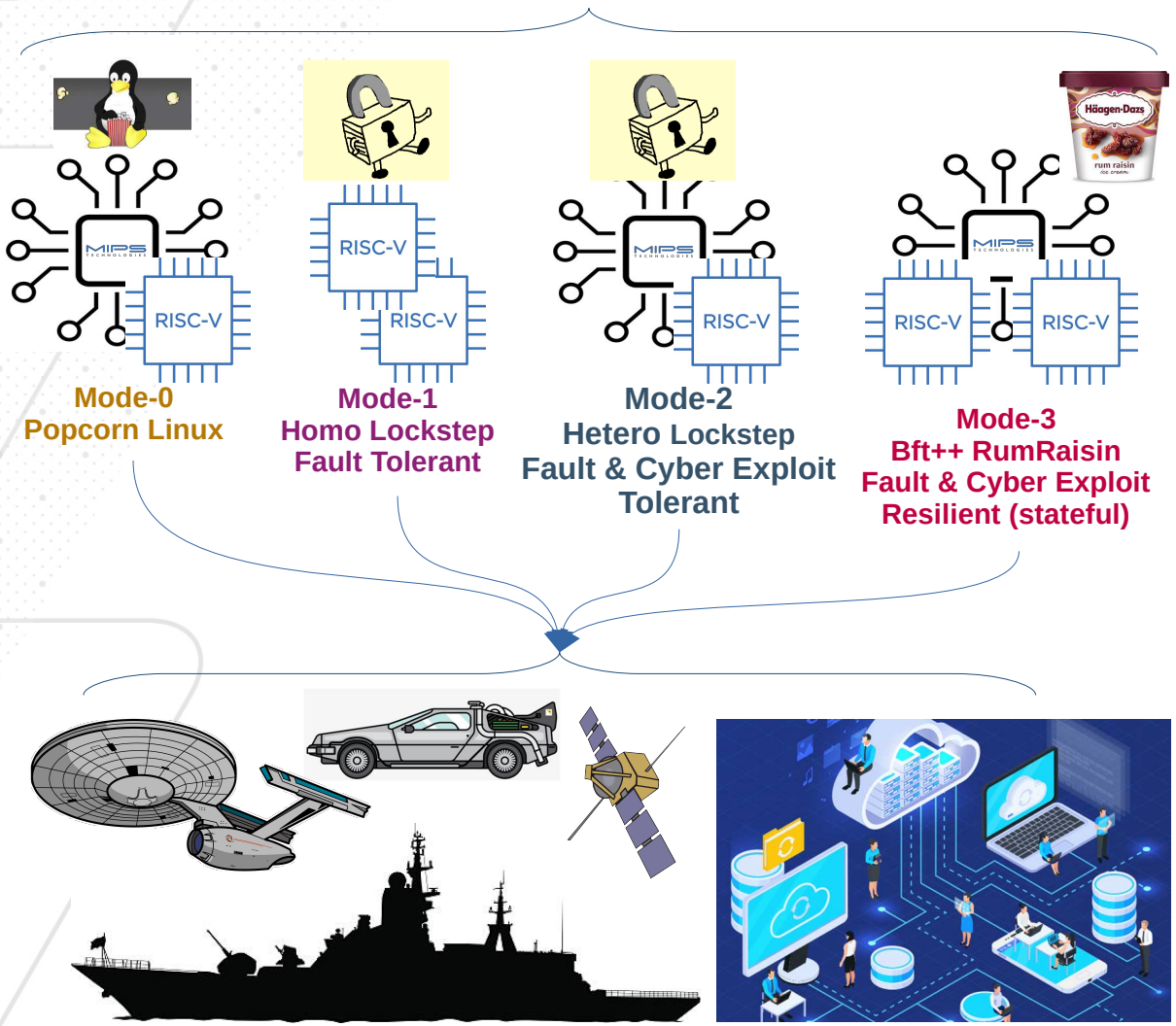
- Dual (homogeneous) Core Lockstep:
  - Highest security ASIL-D in automotive application standard ISO-26262
  - Resilient against Random failure → Fault Tolerant
- However, Dual Homogeneous Cores Lockstep:
  - Susceptible to Cyber-Exploits → Common mode failure
- What is needed is Dual Heterogeneous Cores Lockstep
  - Following the footstep of BFT++ family methods for cyber-attack tolerant
  - Dual Heterogeneous Cores Lockstep is both fault tolerant & cyber-exploit tolerant

Project Proposal (Solution to the problem)

- Develop a proof of concept for Hecocefta, supporting BFT++ v4 (Rum Raisin) on chip
- Employing 3 cores with 2 different instruction set architectures (ISAs); RISC-V and Xilinx's MicroBlaze (or opensource MIPS), 2 RISC-V and 1 MicroBlaze/MIPS
- Provides 4 software configurable modes:
  - Mode-0: simple 3 cores Multi-ISA (2 RISC-V & 1 MicroBlaze), for Popcorn Linux
  - Mode-1: 2 homogeneous core lockstep for ASIL-D (RISC-V)
  - Mode-2: 2 heterogeneous core lockstep for fault & cyber-exploit tolerant version of ASIL-D (RISC-V & MicroBlaze)
  - Mode-3: 3 cores Rum Raisin (BFT++ v4) fault & cyber-exploit tolerant with efficient stateful recovery (2 RISC-V & 1 MicroBlaze) .
  - More ?



Potential Application Areas



- Safety & security critical application and infrastructure where cyber-exploit is a concern
- Applicable to:
- Automotive & Vehicular
- Satellite & Space technologies
- Naval automation & Infrastructure
- Weapon systems
- General IT
- CPS & critical infrastructure
- Etc.

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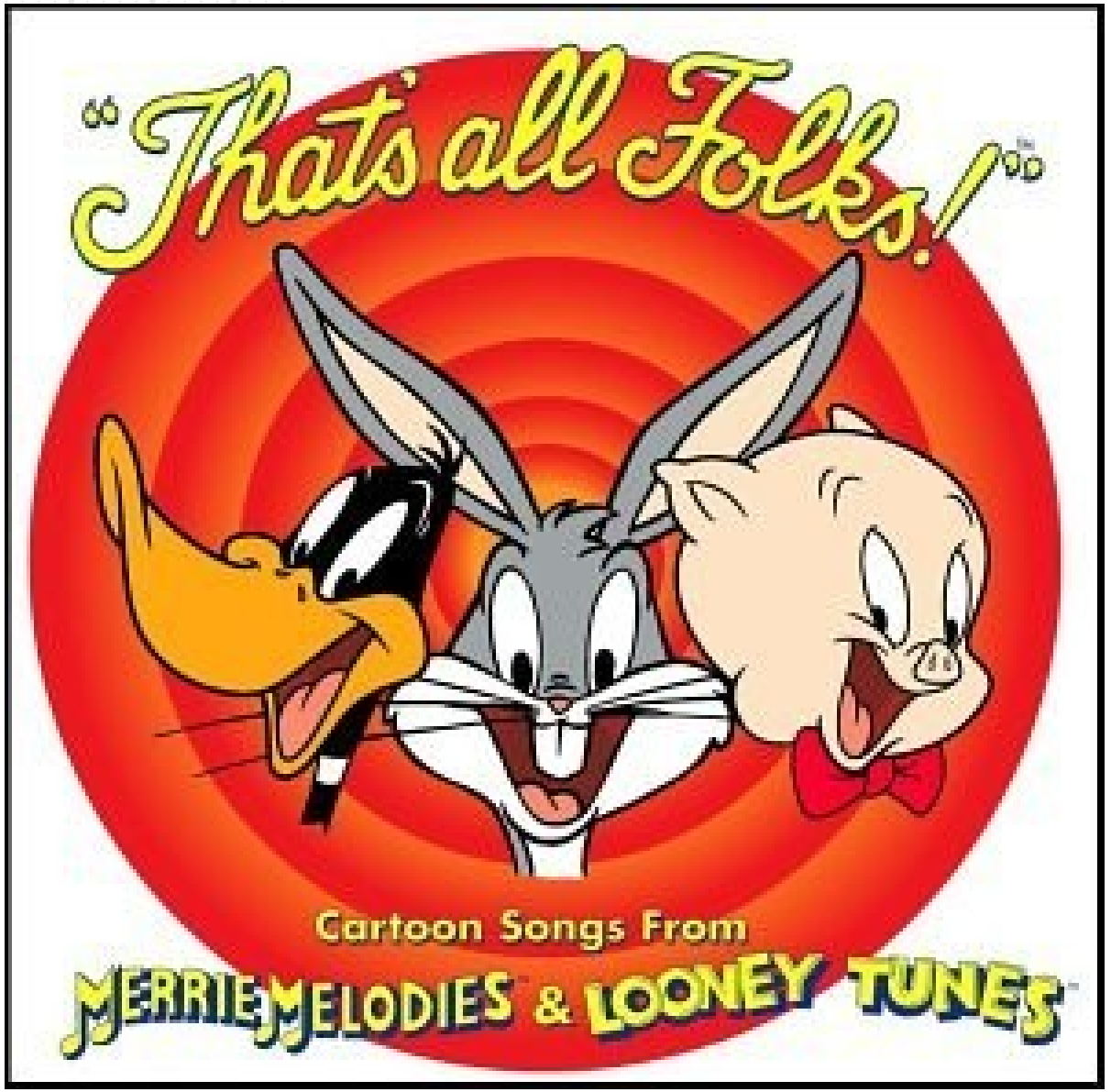

CPS → Physics Rules